ABSTRACT OF THE DISCLOSURE

Before using a netlist description of an integrated circuit as a basis for programming a circuit emulator, a clock analysis tool analyzes the netlist to identify synchronizing circuits including clocked devices ("clock sinks") such a flip-flops, registers and latches for synchronizing communication between blocks of logic within the IC. The tool initially classifies the clock signal input to each clock sink according to its clock domain, sub-domain and phase. The tool then classifies each synchronizing circuit according to relationships between the classifications of the clock signals it employs to clock its input and output clock sinks. The tool then determines, based on the classification of each synchronizing circuit, whether the emulator can reliably emulate that synchronizing circuit, or whether the tool should automatically modify the netlist description of the synchronizing circuit so that the emulator can emulate it. The tool also generates a warning when an emulator may not reliably emulate a synchronizing circuit and the tool cannot automatically modify it so that the emulator can reliably emulate it.